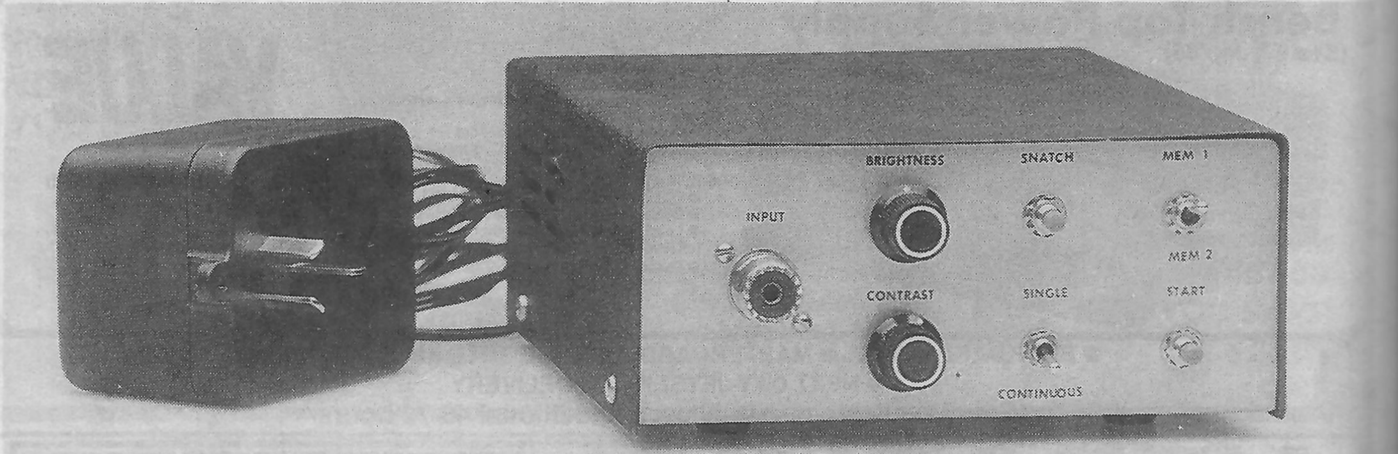
Construction Project:

SSTV Transmit Scanconverter - 1

For many years, radio amateurs have been sending and receiving slow-scan television (SSTV) pictures around the world. Perhaps you're interested in this fascinating mode of communication, and have built or purchased a receive-only scanconverter to 'look in' on the action. Here's a low cost transmit scanconverter design that will allow you to join in, and send your own pictures.

by LEON WILLIAMS, VK2DOB



My interest in slow scan television started about 10 years ago, when I met a fellow amateur who lived nearby. When I heard the tones coming from his transceiver and appearing as pictures on his converted black and white television, I was hooked.

From that moment on, I began building my own scanconverter. Not being very familiar with the concepts I did a lot of reading, searching, asking, building and rebuilding until the day came when my homebrew scanconverter received its first pictures. On a personal level it was a truly momentuous occasion.

The limiting factor was then and has always been the cost and availability of memory chips and analog to digital converters. As these devices became cheaper and obtainable, scanconverters obtained higher levels of sophistication. Today scanconverters are microprocessor controlled and can hold many high definition colour pictures, and rival personal computers in their graphics capability. There is a problem with this situation, however: the complexity of these units is very high. They contain many IC's, some costly and specialised. This unfortunately has prevented a lot of amateurs from home brewing their own.

The project presented here will not equal these units in performance, but will still allow those on a budget to experience the thrill of operating SSTV.

This scanconverter accepts a standard 1V p-p negative sync fast-scan video signal. During the period of one fast scan frame, a portion of 128 lines – which is every second line in a field of 256 lines – is sampled and digitised. This data is written into random access memory (RAM) where it is stored and read out at a slow scan rate. The data is converted to tones and combined with sync pulses to allow correct reception at the distant end.

The unit can store two pictures independently, transmit single frames or transmit continuously, has instant picture 'snatch', camera controls, and as it has its own memory your receive unit can hold pictures while you transmit others.

Inexpensive, easily obtained parts are used and assembly is on two printed circuit boards housed in an inexpensive case. Dangerous voltages are avoided by using a plug pack for the power supply. Construction and alignment are straightforward, needing only basic instruments.

Interested? Well read on, and before long you too, will be sending your own pictures around the world.

SSTV standard

There have been many standards set up over the years for the transmission of SSTV pictures. This unit conforms to the recognised standard for eight second black and white transmission:

Format: 128 dots (pixels) x 128 lines
Shades: 64 (including black and white).
White frequency: 2300Hz
Black frequency: 1500Hz
Horizontal sync: 1200Hz 5ms
Vertical sync: 1200Hz 50ms
Line period: 60ms (55ms active picture plus 5ms horizontal sync).
Frame period: 7.73s (128 line periods plus 50ms vertical sync).

Circuit description

Fig.1 shows the circuit of the fast-scan video amplifier, sync separator and analog to digital converter (ADC) sections. Transistor Q1 is a common emitter input amplifier, with dual supply biasing to allow a large peak to peak signal at its collector. The gain of this stage is about three and the signal is inverted at the collector, with the sync tips being positive going.

The signal is then split into two directions, to Q4 which is the sync separator and also to Q2. Due to the action of C5 and the biasing of Q4, the signal is clamped at such a level that Q4 only conducts on the sync tips and the rest of the signal is ignored. Transistor Q5 is used to buffer and invert the signal so that the horizontal sync signal is a series of positive going pulses. To obtain the vertical sync pulses only, it is necessary to pass the composite signal through an integrator. This is formed with R17 and C13, the resulting vertical sync pulses being buffered and inverted by Q6.

Transistor Q2 has two functions. It is used to amplify the signal by about three times and also to invert the signal so that it is in phase with the input signal. Transistor Q3 follows Q2 and is configured as an emitter follower, with variable biasing provided by the brightness control VR2.

The ADC chip U1 is wired to require an input voltage of OV for black and +5V for peak white. The job of both the contrast and brightness controls is to adjust the signal to fall within these limits. D1 and D2 are used for protection against excursions of input voltage outside the safe range of the ADC.

The ADC used here is an RCA CA3306. It is a 'flash' type, requiring an external clock, has tristate outputs and resolution to six bits. It is perfect for this job and is very reasonably priced.

The input signal is applied to pin 11 and with an input voltage of OV the data outputs D0-D5 will be all low, while with an input voltage of +5V the data outputs will be all high. The data is passed to the tristate output latches on the negative transition of the clock signal at pin 7, while the data outputs are enabled when pin 6 is taken low.

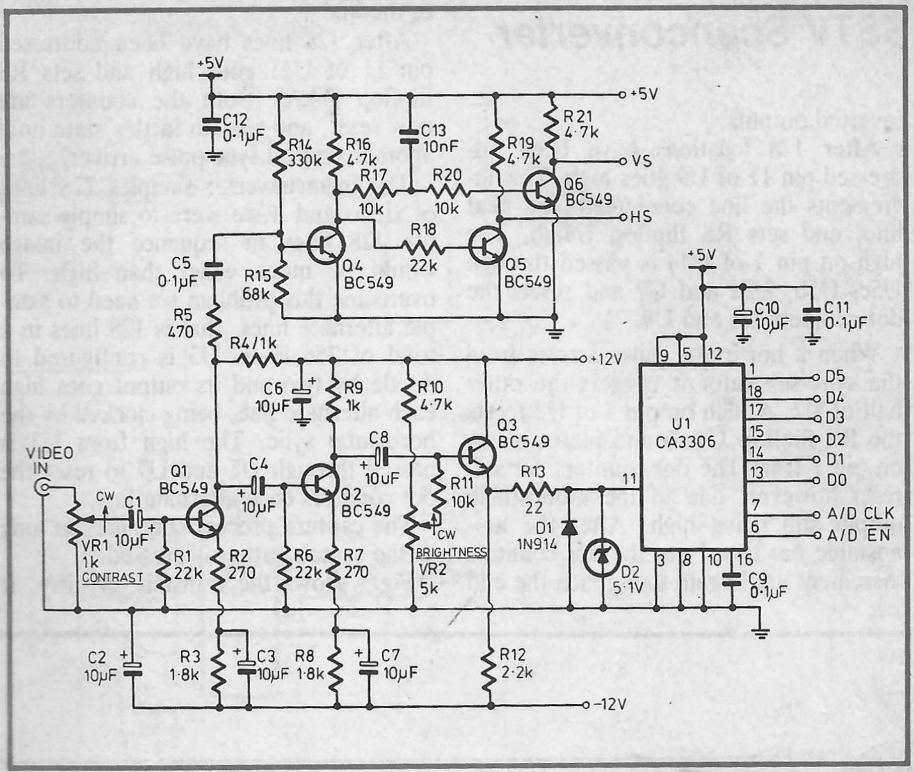


Fig.1: The schematic for the input fast-scan video amplifier, sync separator and analog-to-digital converter sections of the circuit.

Fig.2 shows the circuit of the memory, address, counters, and control logic section. U12 is the picture storage RAM; a 62256 or a 43256 device is used, which is configured as 32K by 8 bits. A slow scan picture is 16K, so that we can store two pictures. Pin 21 is used to select the half required and effectively becomes the most significant address bit.

You may have noticed that the ADC has a resolution of only six bits and therefore one quarter of the RAM IC is unused. While this is wasteful, it is much easier to employ this scheme than to use six dynamic RAM IC's and the refresh circuits they would require. U8 and U9 are the dot counters and keep track of the dots in a line. U10 and U11 are the line counters. Both dot and line counters can address a maximum of 128 locations.

U6 is the fast scan clock source. The crystal chosen is a common type and as a bonus results in a near 1:1 aspect picture. U7, a 74LS158, is effectively a four pole double throw switch. In the snatch mode it selects the counter resets, clock and memory write pulses from the control circuit. In the transmit mode it selects counter resets and clock from the transmit circuit. U2 is a dual monostable which is used to delay the digitising process from the top and left of the frame, to centre the sampling 'window' in the fast-scan frame.

The operation of the control circuitry may not be obvious at first, so let's have a closer look. Once the snatch button has been pushed, U7 selects the control circuit signals. Upon a vertical sync pulse arriving from the sync separator it triggers one half of U2. This causes the Q output at pin 13 to go high, resetting the RS flipflop U4c/d and placing a low on pin 9 of U5d. Pin 8 of U5d is held high however by U2 pin 13 still being high. The high is passed through U5b, U5a and U7 to reset the dot counters, U8 and U9, and by pin 11 U7 to reset the line counters U10 and U11. We have therefore all counters reset, addressing the first dot in the first line after a delay following a vertical sync pulse.

Once the vertical sync delay has ended pin 8 U5d goes low, allowing the dot counters to increment. The crystal clock source is used to clock the dot counters and the ADC on the negative transition. The memory is placed in write mode and the ADC tristate outputs are enabled when the clock is in the low state.

In the transmit mode the ADC's outputs are placed in a high impedance state and the memory is placed in permanent read mode. Note that U7 has inverted outputs.

After 128 locations have been addressed pin 11 of U9 goes high. This increments the line counters to the next line, and sets RS flipflop U4a/b. The high on pin 1 of U4a is passed through U5c, U5b, U5a and U7 and resets the dot counters U8 and U9.

When a horizontal pulse arrives from the sync separator it triggers the other half of U2. A high on pin 5 of U2 resets the RS flipflop U4a/b and places a low on pin 1 U4a. The dot counters are still reset however, due to the monostable output still being high. After the monostable has timed out the dot counters increment until again they reach the end of the line.

After 128 lines have been addressed pin 11 of U11 goes high and sets RS flipflop U4c/d. Both the counters are now reset, and remain in this state until another vertical sync pulse arrives.

This scanconverter samples 128 lines of video and if we were to simply sample 128 lines in sequence the image would be much wider than high. To overcome this problem we need to sample alternate lines, that is 128 lines in a total of 256 lines. U3 is configured to divide by two and its output goes high each alternate line, being clocked by the horizontal sync. The high from U3 is passed through U5 and U7 to reset the dot counters each alternate line.

The capture process continues as long as the snatch button is pressed.

Fig.3 shows the transmit circuitry. It can be broken into two separate parts, the sync generator and the digital to frequency converter.

Firstly to the sync generator. At the end of a line one half of U13 is triggered at pin 10 to produce a 5ms horizontal sync pulse at pin 5, which resets the dot counters via U14c and U14d. At the end of a frame the other half of U13 is triggered at pin 2, to produce a 50ms vertical sync pulse at pin 13 which resets the line counters directly and the dot counters via U14c and U14d. Either sync pulse produces a low on U14c pin 13 to reset the slow-scan clock generator U15.

A 555 is used here in the astable mode, with pin 4 used as a reset. The clock is reset during sync pulses to ensure that it is in the same phase at the start of each line. The clock generator is

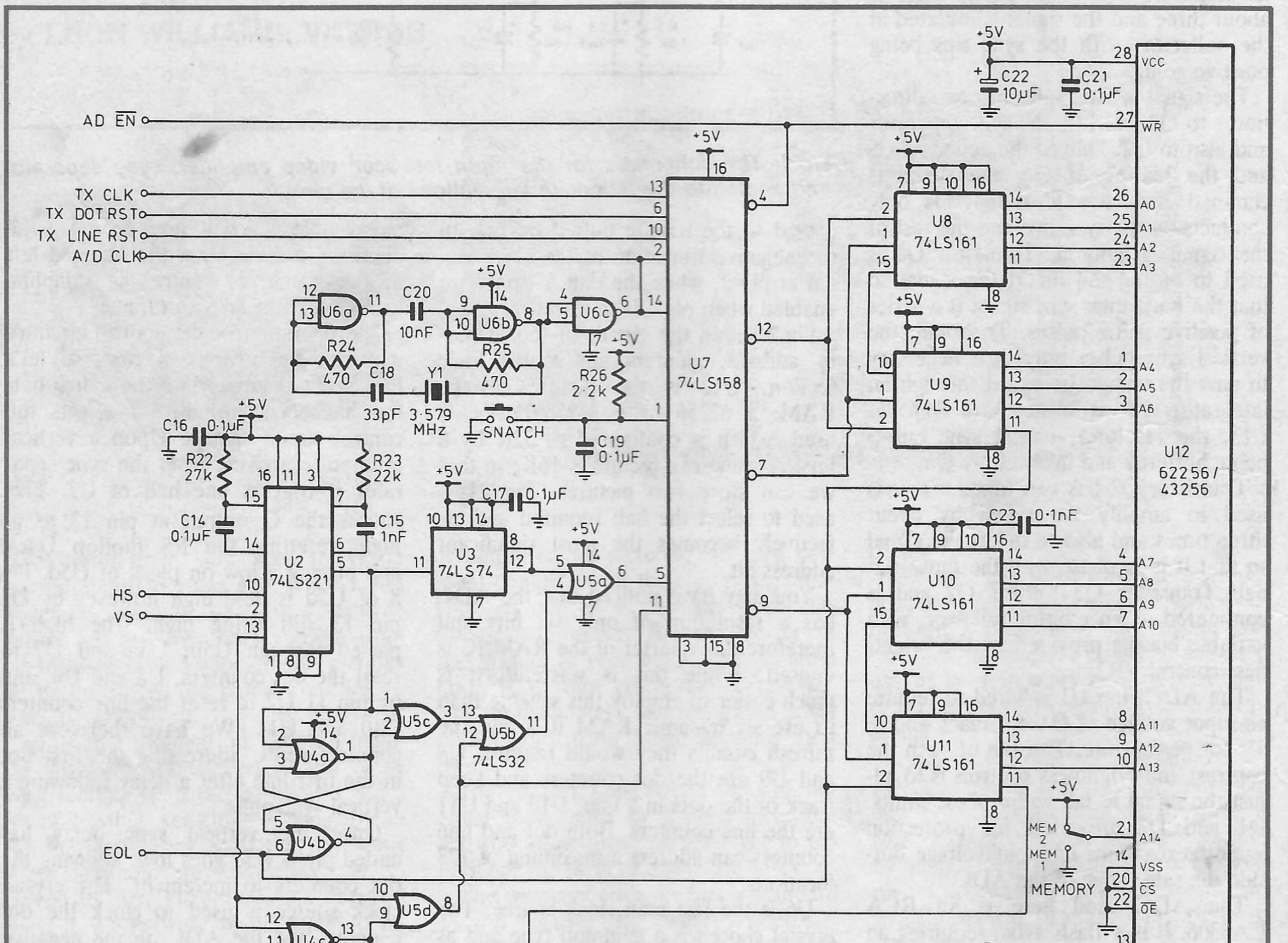


Fig.2: The schematic for the memory, address, counters and control logic circuits.

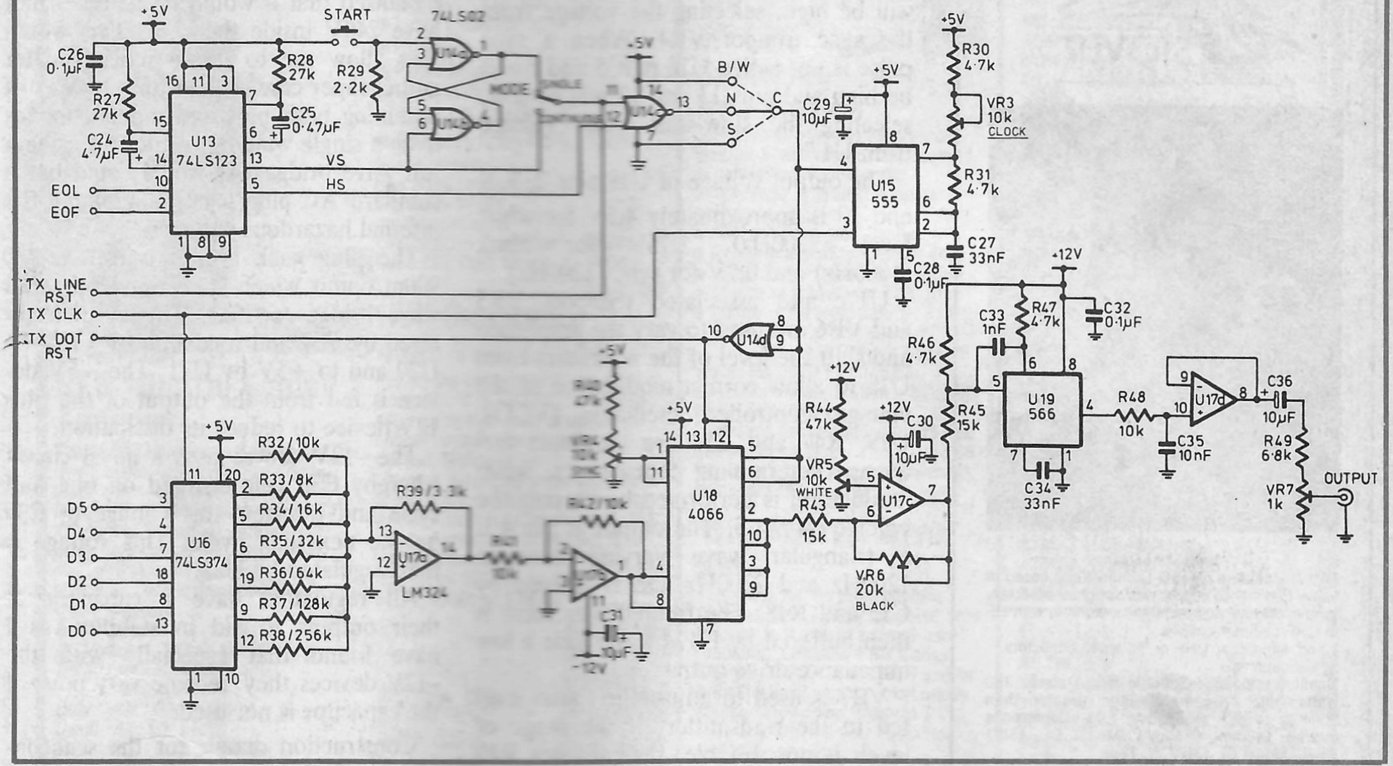


Fig.3: The slow-scan transmit circuitry. U15 is the slow scan clock generator, U16 with its resistors perform D to A conversion, and U19 the audio frequency modulation.

adjusted for a frequency of approximately 2327Hz. This is calculated by dividing the active line period of 55ms by 128 dots. The output at pin 3 is used to increment the dot counters on the negative transition and latch the data by U16 on the positive transition.

With the single/continuous (mode) switch in the single position, a vertical sync pulse will set the RS flipflop formed by U14a/b, to produce a high on pin 1 U14a. This high on pin 11 U14c causes a permanent transmission of 1200Hz sync tone. When the start switch is pressed the flipflop is reset and picture transmission commences from the top of the frame. At the end of the frame another vertical sync pulse again sets the flipflop and only sync tone is transmitted.

With the switch in the continuous position, the start switch is not used, and when the bottom of the frame is reached a vertical sync pulse is transmitted and the picture continues from the top of the frame and repeats indefinitely.

U13 is a retriggerable monostable and is used because during snatch periods the EOL and EOF lines will be pulsing. If we used a non-retriggerable monostable the outputs of U13 would not be in a permanent state and would cause spurious signals to be transmitted.

If a picture is being transmitted and the snatch button is pressed, the transmission will stop and a permanent 1200Hz will be sent with the mode switch in the single position. With the switch in the continuous position, pushing the snatch button during transmission will cause 1200Hz to be sent while the button is pressed and the frame will start from the top again after the button is released.

Now we will look at the digital to frequency converter. As the memory address counters are incremented, the corresponding memory data will appear at the inputs of U16, which is used here as a six-bit latch. A 74LS374 was selected because of its high output drive capability, and so its tristate outputs are permanently enabled. A digital to analog converter is formed with U16, a set of binary weighted resistors, U17a and U17b.

R32 is used to bias the output voltage of U17b above OV. U18 is wired as a single pole double throw analog switch. When a sync pulse is active U18 pins 5 and 6 will be low, and pins 13 and 12

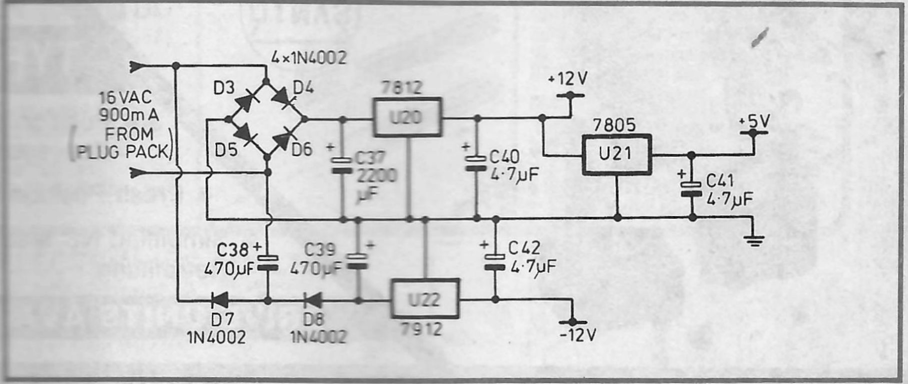


Fig.4: The power supply section, which produces the necessary +12V, –12V and +5V from an external 16V AC plug pack.

will be high, selecting the voltage from the sync trimpot VR4. When a sync pulse is not active U18 pins 5 and 6 will be high and pins 13 and 12 will be low, selecting the slow-scan video voltage from U17b.

The output voltage of U18 pins 2, 3, 9 and 10 is approximately 4.5V for white level (2300Hz), 1.75V for black (1500Hz) and 0.7V for sync (1200Hz).

U17c and associated trimpots VR5 and VR6 are used to vary the amplitude and shift the level of the waveform from U18 to allow correct modulation of the voltage controlled oscillator (VCO), U19. R47 and C34 are the main frequency determining components, while modulation is performed by varying the voltage on pin 5. The output at pin 4 is a triangular wave varying between 1200Hz and 2300Hz and is filtered by C35 and R48. The filtered waveform is then buffered by U17d to provide a low impedance drive output.

VR7 is used to adjust the audio level fed to the transmitter. If the range of levels is not suitable, then resistor R49 should be adjusted to suit.

The power supply circuit is shown in Fig.4. I originally designed the power supply around a conventional centre-tapped transformer. After some thought I realised that it would be better to not have 240V inside the case. This would also allow me to use a much smaller and cheaper case. I then found a way of obtaining both plus and minus supplies from a single winding, while still using a full wave bridge. As well I could use a standard AC plug pack, eliminating the internal hazardous voltages.

The plug pack I used is a 16V AC 900mA unit which is rectified by a full wave bridge rectifier. This is then filtered by C37 and regulated to +12V by U20 and to +5V by U21. The +5V device is fed from the output of the plus 12V device to reduce its dissipation.

The –12V source uses a novel circuit whereby C38 gets charged on one half cycle and transfers this voltage to C39 on the next half cycle. This voltage is then regulated by U22.

All regulators have a capacitor at their outputs to aid in stability, as I have found that especially with the –12V devices they become very noisy if the capacitor is not used.

Construction details for the scanconverter will be given in the second of these articles, along with its testing and alignment. EA