# Color Computer SSTV: Part I

*Turn your CoCo into a complete SSTV terminal! How? First, build this high-resolution display system.*

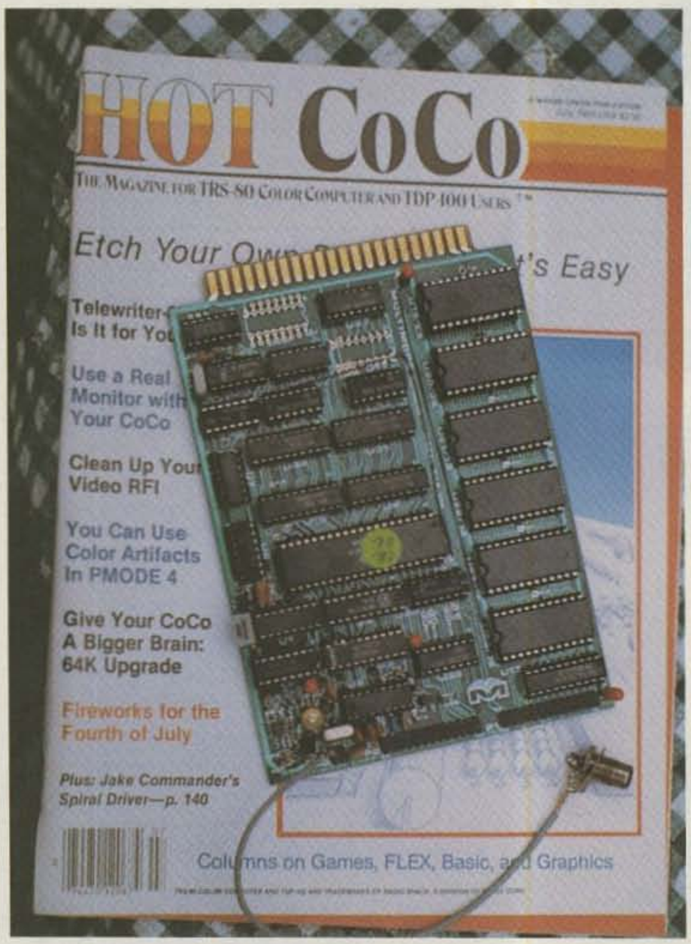


Photo A. Multimode display board, showing the physical size of a production display interface. The board has 16K of display memory.

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This two-part article describes a high-resolution display system for the Radio Shack Color Computer® (CoCo). This system provides the CoCo computer with more display capability than any low-cost computer. You might ask why you should use your CoCo to display and generate television images. One answer is, for communications.

Imagine taking your CoCo with a hardware-software interface and connecting it to amateur-radio equipment and transferring a picture to

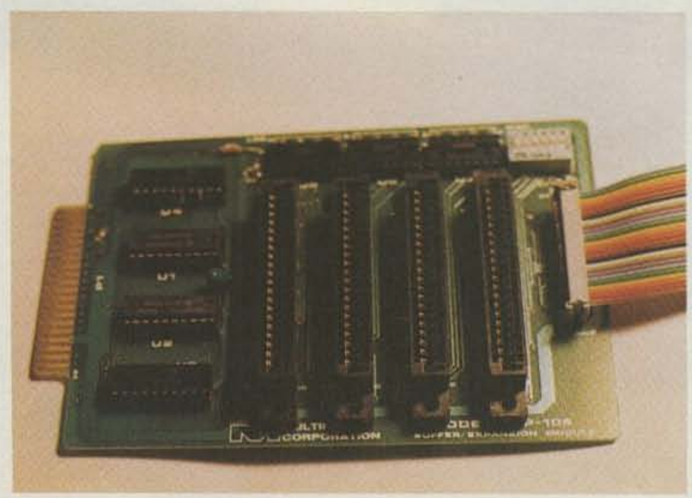

Photo B. Multimode CoCo interface board, which plugs into the expansion interface of the CoCo. A 26-pin flat cable interconnects the interface board and the display board.

someone miles away, or receiving weather-satellite pictures. The digital-television-display field is one which has not been explored by the amateur-computing community, and only a small amount of commercial equipment exists for such applications. In this article, instructions will be provided to construct a card to display high-resolution images and provide interfaces to receive weather-satellite pictures or amateur-radio SSTV.

Before plowing ahead with a lot of technical jargon and confusing terms, some definitions are in order.

**Background**

In display terminology two terms are particularly important. These terms are used also in television. The first is pixel, and it relates to the smallest element of a picture which can be seen on the TV screen. In normal TV, the pixels are so small that they tend to blend together to form a contiguous image. In digital TV, a pixel is a unit in the picture which can be seen by the unaided eye. Each pixel in digital TV has an intensity or discrete color. The main goal in digital TV is to place the most pixels on a line to form the smoothest image. To do this as well as standard TV does takes a lot of complex and costly circuitry.

The second term is number of lines per picture. In the USA, standard TV has 262 lines per frame or 525 lines per interlaced picture. In digital TV, the number of lines is often reduced from normal TV for cost and simplicity reasons.

If a digital-display system could be developed around a standard microprocessor system, the system would be very versatile. The few commercial display systems which have been developed to date have some disadvantages.

*Expandability.* Microprocessors have been installed in some of the new display-system designs. All of these units are not user-programmable. Most vendors would rather provide users with new units when their function is to be expanded. If a system were to be based on a commercial microprocessor with a good software base, the system could be expanded as technology progresses.

*Fixed Architecture.* Most commercial systems are built around a large planar board with lots of ICs and discrete components. These units are designed for a specific application and a limited life span. Adding interfaces like FAX and other applications is difficult. For this reason, the modular approach of functional units connected to a microprocessor makes good sense.

Up to a few years ago, digital TV was not possible. With the explosion of the semiconductor industry, the price of ICs has fallen to a level which makes this economically possible. Most of the early digital TV scan converters used were hardware-only devices. These units were very dumb and could only generate and display images. The explosion of digital computers and the incorporation of digital displays in computers makes the whole concept very exciting. Once an image is placed in the computer, almost anything is possible: communications, image analysis by computer for manufacturing inspection, medical applications, or art forms for their own sake.

Two applications will be described in this article. The first application is amateur-radio slow-scan television; the second is weather-satellite reception. While the applications are similar in that they require some means of picture displaying and a

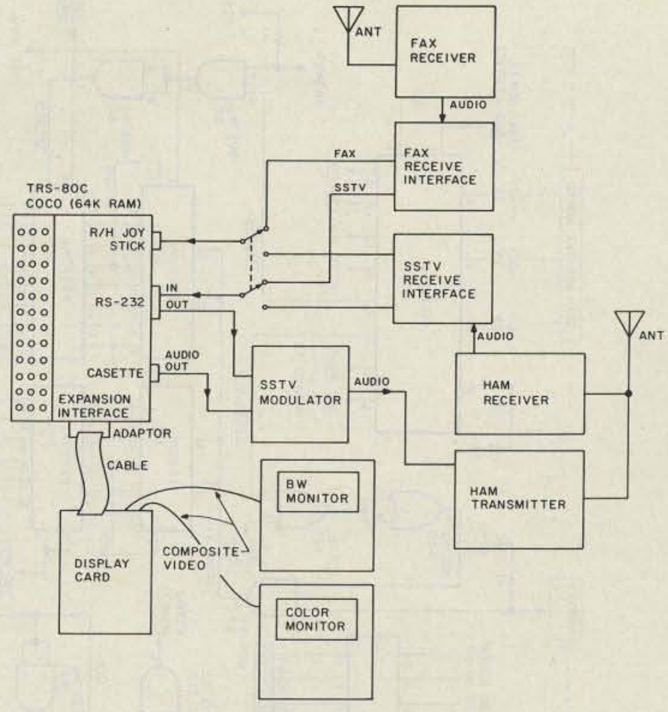


*Fig. 1. System block diagram, showing the interconnection of the computer and all the interfaces.*

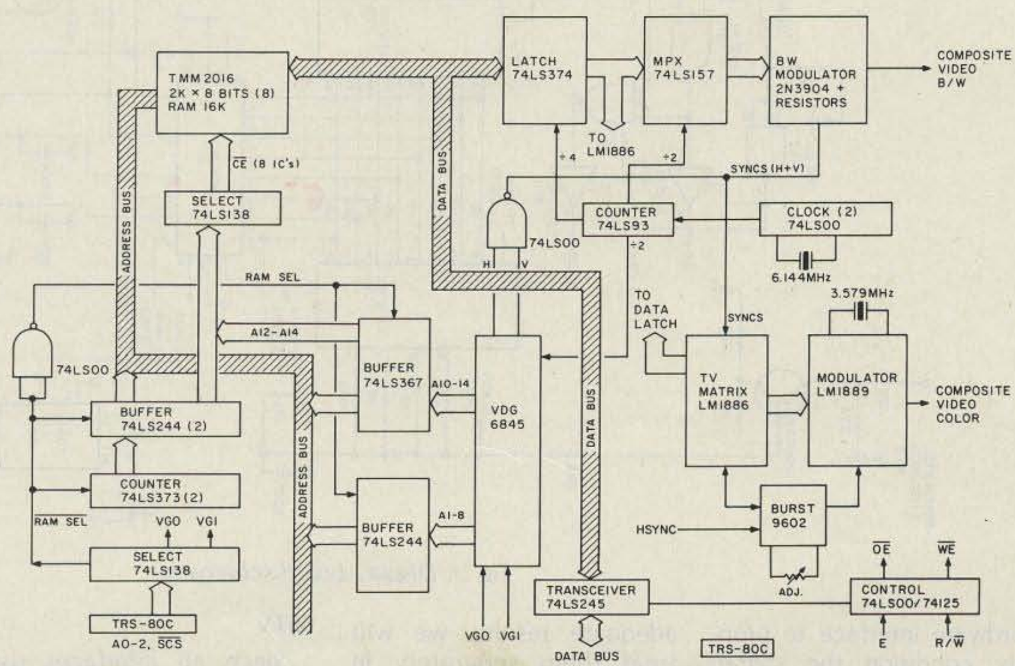


*Fig. 2. Display block diagram, showing how the display interface functions. Only the important ICs are shown.*

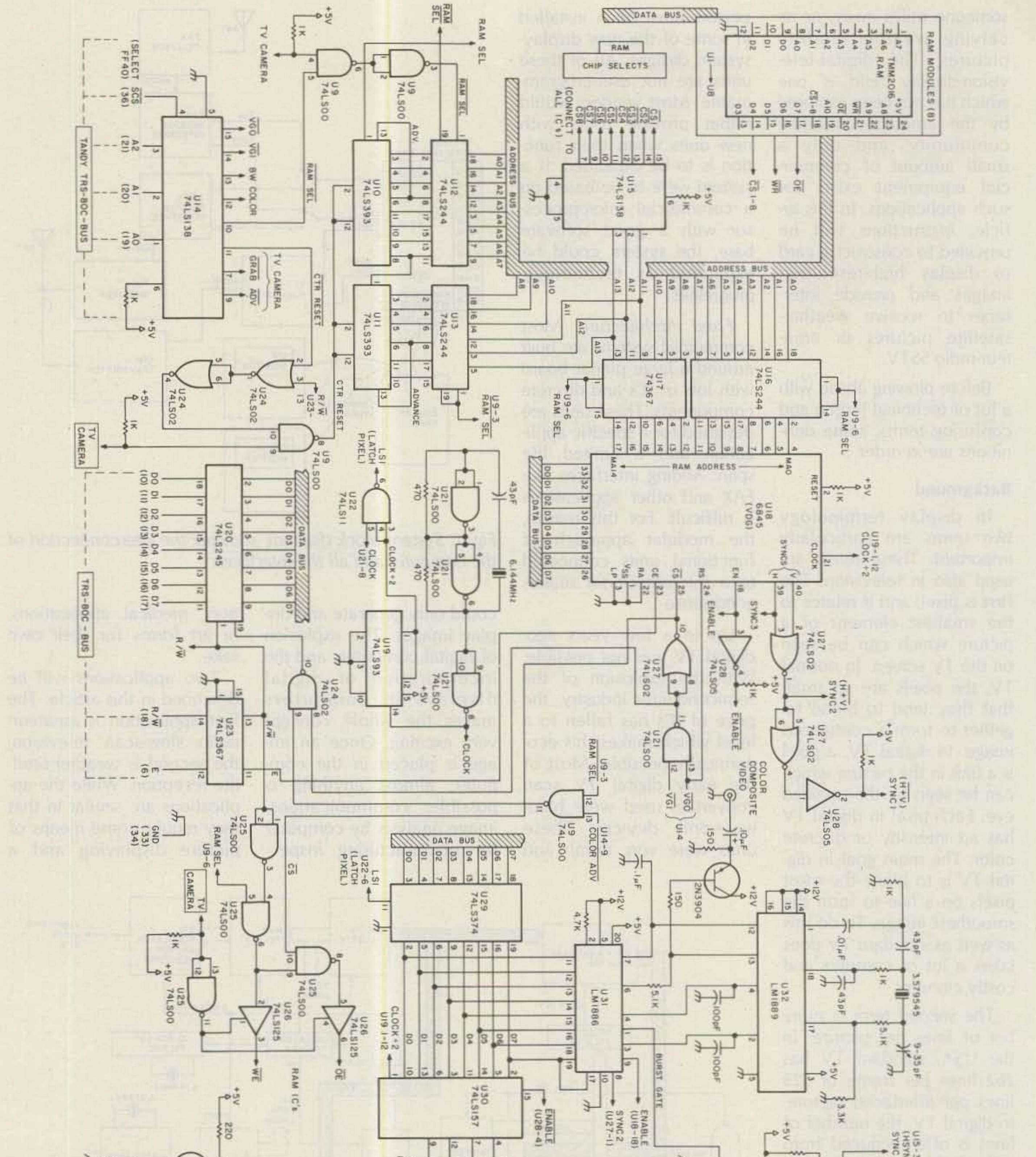


*Fig. 3. Display board schematic.*

hardware interface to properly condition the signal, and each requires trade-offs and compromises to achieve adequate results, we will treat them separately in order to do an adequate job on each.

**SSTV**

Since all interfaces use simple hardware, the heart of the system is software. It would be impossible to publish an entire software package in an article of this type. To date, thousands of lines

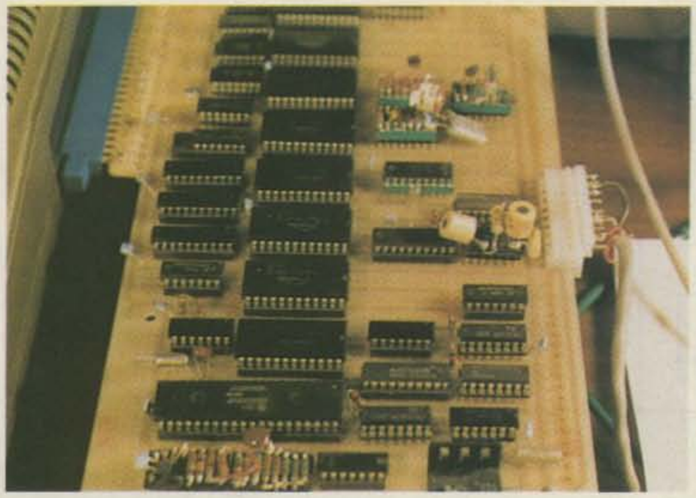

Photo C. The prototype board by K6AEP was one of the first display boards constructed. The board is plugged into a CoCo. The board was point-to-point wired and is exactly like the schematic in Fig. 3. All of these photos in part I of this article were generated by this board. The same results can be achieved by the commercial display boards.

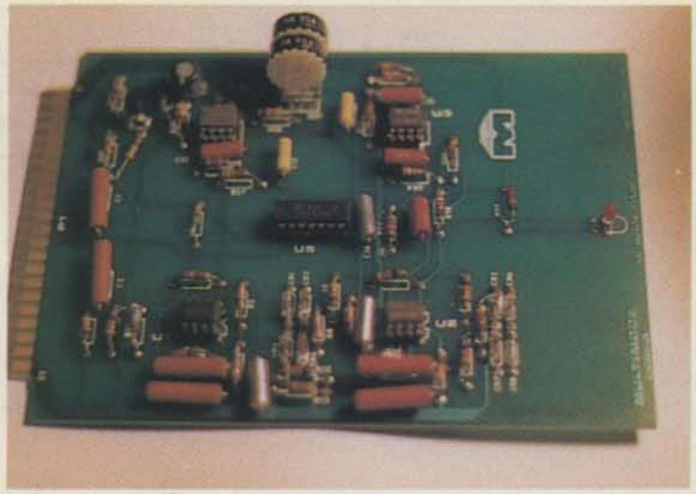

Photo D. A multimode SSTV receive interface. This board is a commercial version of the SSTV receive interface. The physical size is the same as the display board.

of code have been developed. What will be provided here is a technical description of how the software and hardware interfaces function and the steps necessary to develop code. You will find it possible to modify the concepts we present for interfacing with any microprocessor system.

### The Display Criteria

Since the main goal of the display card is to produce quality images, it is important to make the picture density as high as possible. This requires the addition of RAM memory in which the image will be saved and displayed. Experimentation by many people over a period of years has determined that a minimum of 128 pixels per line is required for low-resolution images, with at least 16 gray levels. Some experimentation which I conducted in mid-1982 indicated that a minimum of 256 colors per pixel is required to display low-resolution color-TV images.

Armed with this information, a design criteria of 256 pixels per line, 16 gray levels, on 128 lines was defined for black and white displays. This equates to a display size of 16K of display RAM. With a little clever programming and slight reconfiguration of data bits, a total of 256 colors can be displayed for each pixel with 128 pixels per line on 128 lines.

Obviously, a system can be constructed with higher resolution, but as the digital-display density increases so do the cost and complexity. Since this project was created for the average hobbyist with a limited budget, the above criteria seem adequate for today's technolgy.

### Hardware Design

It is unfortunate that no off-the-shelf module or design provides the necessary ingredient to display TV-type images. Many manufacturers have developed display-controller ICs for computer terminals, but in most cases they are unusable in TV applications. One of the few ICs which make the job easier is the Motorola 6845. This IC is the heart of the display board and causes the image to be displayed.

The card is designed to attach to the Radio Shack TRS-80C Color Computer, but the design concept is so basic that it can be altered to attach to any microcomputer. The card functions by first generating or placing an image in the main memory of the computer. The TV image can be received through a slow-scan demodulator attached to the receiving equipment then connected to the joystick input of the computer.

Another method of image generation is to attach a special hardware interface to the display card and frame-grab the image into the display card from a TV camera. At this time the TV-camera interface has not been developed. When using the TV camera, the image will be loaded into the video card first and then transferred by computer software to main memory.

### System Description

Fig. 1 provides a block diagram of the entire system. The TRS-80C in this application acts as an intelligent controller. All interfaces are very primitive and cannot function without intensive control from the computer. When an image is to be displayed from the receiver, the audio tones are first detected by the display demodulator and converted to two types of signals: sync pulses and a dc voltage which changes as a function of the input audio frequency. These signals are connected to the CoCo's RS-232 input and the joystick input.

The joystick input is actually an analog-to-digital converter which can be used to digitize slow-scan TV video into picture information. All of the operation is controlled by software in the CoCo. When digitized, the pixels are transferred to the display card and immediately displayed. For transmission, the image is first created by software and placed in the CoCo's memory. To transfer the image to a transmitter, the sync pulses are controlled by the RS-232 output line and the video is controlled by the computer's cassette output, which is a digital-to-analog converter.

The above process is true only for black and white television. Color digital TV is more complex. Color TV is developed or transferred from three image planes. Each plane consists of the three prime colors (red, green, and blue). When the three frames are mixed together, a color image is formed. The image can then be transferred to the display card. The transmission method of colored television is either by frame-sequential or by a colored line-sequential multiplexed method.

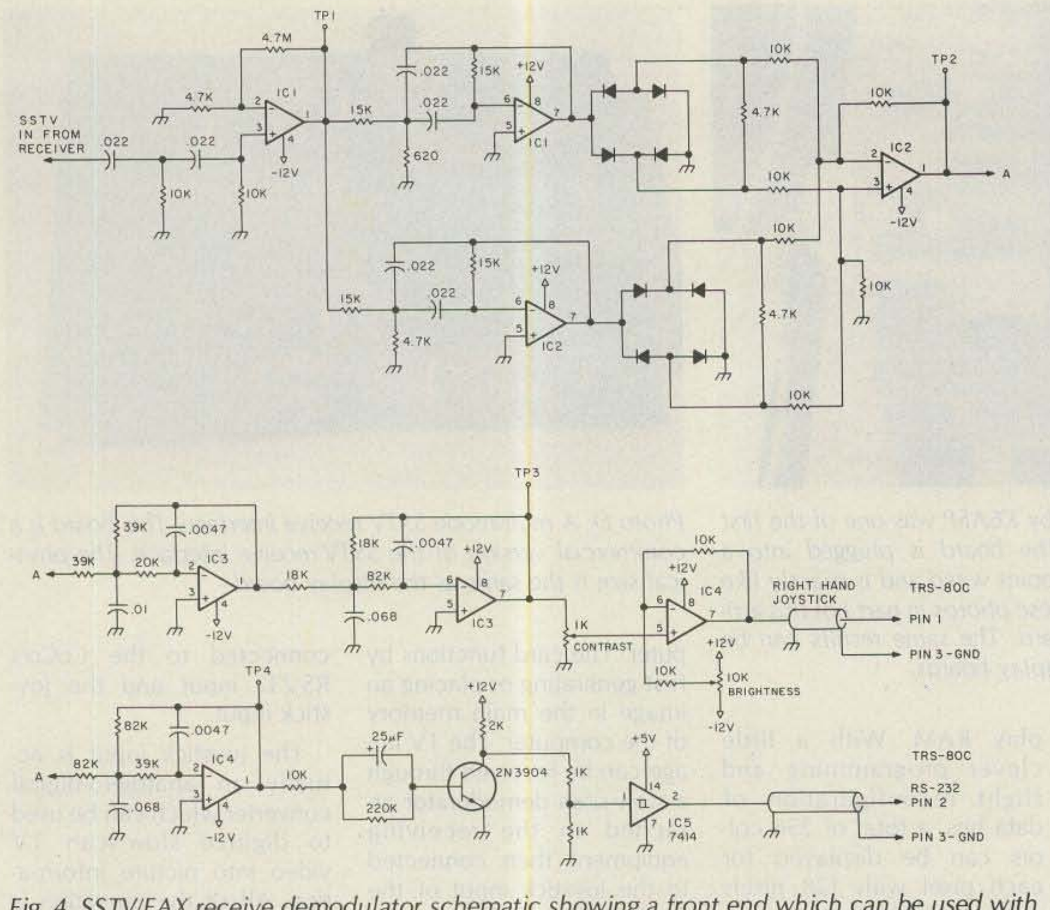


*Fig. 4. SSTV/FAX receive demodulator schematic showing a front end which can be used with the computer to display both SSTV and FAX images. The FAX application can be used only on the HF bands.*

The block diagram of the display card is shown in Fig. 2 and the schematic is shown in Fig. 3. The following sections describe the major functional parts of the display board.

**Display Board**

The display board is attached to the expansion port on the side of the CoCo. This port provides connection to the address, data, and control signals of the 6809E MPU. Wiring to the CoCo must be as short as possible; less than one-half-inch leads are a must. The data lines are connected to both the eight RAM ICs and the VDG U18 (6845) display-controller IC through a data bus transceiver (U20). The R-W line determines if the CPU is reading or writing to the board.

In order for the display-controller IC to function, you must first write data to its 18 internal registers. Only three address bits of the 6809 CPU IC are connected to the card. These low-order address bits select the mode which you are performing. The SCS line on the TRS-80C connector is used to select address FF40. The interface E line is the enable signal from the 6809 CPU. This line is used to synchronize the 6845 to the CPU IC for writing to its internal registers.

1. *Functional Selection.* All internal functions of the card are software-selected by a U14 (74LS138). The functions are shown in Table 1 and are described in more detail in the programming section of this article.

2. *Random Access Memory.* This card contains 16K of display RAM (U1 to U8) in eight 2K-by-8-bit ICs. Static RAM was used so as to make the design as simple as possible. Dynamic RAM has the advantage of lower cost but requires extra circuitry to develop RAS and CAS signals, and it is difficult to correct and diagnose problems when they occur. Simple changes can be made to the circuit to add more display memory. Modifications have been made to add 32K RAM. The board can then display 256 pixels on 256 lines, black and white. Television pictures in this mode are starting to approach standard US TV quality pictures.

Control of read or write to the RAM is determined by U25 and U26. During most of the time, RAM is in the read mode. This causes the video data to be valid on the internal data bus. When data is written, it is transferred to and from the CoCo through bus transceiver U20 to the RAM ICs.

3. *Video Display Generator.* The VDG U18 is the heart of the display board. This integrated circuit has 18 registers. In order to make the board operational, the registers must be preloaded before a picture can be displayed on the card. This IC is used to develop the video refresh timings of the RAM. By simply changing the initialization values, either 50-Hz or 60-Hz video can be displayed.

An example of CRT initial-

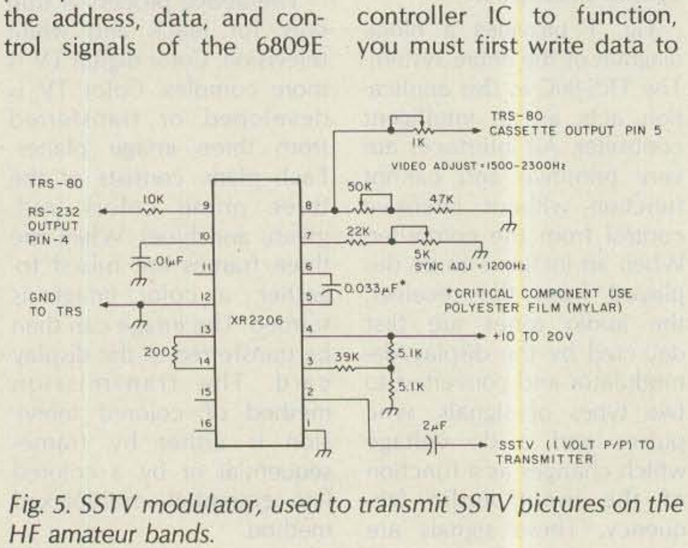


*Fig. 5. SSTV modulator, used to transmit SSTV pictures on the HF amateur bands.*

| ADDRESS | SIGNAL |
|---|---|
| FF40 | VG0 VDG controller address register |
| FF41 | VG1 VDG controller data register |
| FF42 | Spare |
| FF43 | Spare |
| FF44 | Reset—reset RAM address counter |
| FF45 | Select—send picture data to card |
| FF46 | Frame Grab—TV camera—reserved |
| FF47 | Color—TV camera—reserved |

*Table 1.*

```
                  * ASSEMBLER EXAMPLE FOR CODING A PROGRAM
                  * TO RECEIVE SSTV OF FAX WITH A TRS-8ØC
                  * COLOR COMPUTER
                  *
                          OPT PAG
Ø6ØØ                      ORG $Ø6ØØ
                  * EQUATES
             FF45 PORT2   EQU $FF45     DISPLAY A PIXEL
             FF44 PORT3   EQU $FF44     RESET HARDWARE COUNTER
             1ØØØ START   EQU $1ØØØ     DUMMY START ADDRESS FOR PICTURE INFO

Ø6ØØ BE   1ØØØ    RECV    LDX #START    START OF PICTURE IN RAM
Ø6Ø3 BD   49              BSR INIT      INITALIZE MPX IN TRS-8ØC
Ø6Ø5 86   8Ø              LDA #128      256 PIXELS PER LINE
Ø6Ø7 B7   Ø651            STA PIXC      PIXEL COUNTER
Ø6ØA B7   Ø652            STA LINE      LINE COUNTER
Ø6ØD B7   FF44            STA PORT3     RESET COUNTER ON DISPLAY CARD
                  *
Ø61Ø 8D   3B              BSR VSYNC     WAIT FOR VERT SYNC
Ø612 8D   37      RECV1   BSR ADC       GET A READING FROM COCO ADC
Ø614 12                   NOP           EQUALIZE CYCLES TO KEEP
Ø615 12                   NOP           SOFWARE JITTER TO A
Ø616 12                   NOP           MINIMUM
Ø617 12                   NOP
Ø618 12                   NOP
Ø619 12                   NOP
Ø61A 34   Ø2              PSHS A        SAVE ADC ON THE STACK
Ø61C 1ØBE Ø64F            LDY DELAY     PLACE DELAY CONSTANT IN Y
Ø62Ø 31   3F      RECV2   LEAY -1,Y     DELAY LOOP BETWEEN PIXELS
Ø622 26   FC              BNE RECV2
Ø624 44                   LSRA          FORMAT PIXEL INTO RIGHT
Ø625 44                   LSRA          NIBBLE (4 BITS)
Ø626 44                   LSRA
Ø627 44                   LSRA
Ø628 AA   EØ              ORA Ø,S+      ADD PIXELS
Ø62A 1ØBE Ø64F            LDY DELAY     DELAY CONSTANT
Ø62E B7   FF45            STA PORT2     DISPLAY TWO PIXELS
Ø631 A7   8Ø              STA Ø,X+      PLACE A COPY IN RAM
Ø633 31   3F      RECV3   LEAY -1,Y     DELAY LOOP
Ø635 26   E9              BNE RECV2
Ø637 7A   Ø651            DEC PIXC      DECREMENT PIXEL COUNTER
Ø63A 86   8Ø              LDA #128      RE-INT PIXEL COUNTER
Ø63C B7   Ø651            STA PIXC
Ø63F 26   D1              BNE RECV1     DO IT TILL LAST PIXEL
Ø641 7A   Ø652            DEC LINE      IS IT LAST LINE ?
Ø644 27   Ø4              BEQ END       DO IT TILL LAST LINE
Ø646 8D   Ø4              BSR HSYNC     WAIT FOR HORIZONTAL SYNC
Ø648 2Ø   CB              BRA RECV1     DO IT ALL OVER AGAIN
                  *
                  * END THE WHOLE PROCESS
                  *
Ø64A 39           END     RTS           RETURN TO MAIN LINE CALL
                  *   ADC ROUTINE- RECEIVE A PIXEL THROUGH ADC PORT
                  *   JOYSTICKS - PERSERVE THE X AND A REGISTERS
                  *   RETURN WITH ADC VALUE IN A
                  *
Ø64B 39           ADC     RTS           DUMMY RETURN
                  *
                  *    SYNC ROUTINES- SAMPLE RS-232 INPUT PORT AND WAIT FOR
                  *    THE INPUT TO RISE THAN FALL. VERTICAL SYNC SHOULD
                  *    LOOK ONLY FOR PULSES GREATER THAN APPROXIMATELY 3Ø
                  *    MILLISECONDS. IF THE PULSE WIDTH IS LESS THAN APPROX.
                  *    3 MILLISECONDS THEN IT IS A HORIZONTAL SYNC PULSE.
                  *
Ø64C 39           HSYNC   RTS           DUMMY H SYNC
Ø64D 39           VSYNC   RTS           DUMMY V SYNC
                  *
                  * INITALIZE MULTIPLEXER IN COCO TO CONNECT JOYSTICK
                  * INPUT TO THE CORRECT PIN ON THE CONNECTOR. JOYSTICK
                  * INPUTS CAN BE A POSSIBILITY OF 4 PINS
                  *
Ø64E 39           INIT    RTS           DUMMY MPX SELECTION
                  *
                  *  DELAY- CONSTANT TO ALLOW FOR DELAY BETWEEN PIXELS
                  *  VARIABLE TO COVER ALL MODES OF RECEPTION
                  *
Ø64F ØØ1Ø         DELAY   FDB $ØØ1Ø     SAMPLE DELAY
                  *
                  * GENERAL STORAGE FOR PROGRAM CONSTANTS
Ø651 ØØ           PIXC    FCB Ø         PIXEL COUNTER DELAY
Ø652 ØØ           LINE    FCB Ø         LINE COUNTER DELAY
                  *
                          END RECV
```

*Fig. 6. Program example for SSTV/FAX receive, written in 6809 assembler language, to demonstrate how easily a receive routine can be written. The routine cannot be executed without software additions.*

ization is contained in the programming section. The initialization constants were chosen to display an image with the minimum amount of tearing and proper centering on a 9-inch RCA Color Trak TV set. The TV set was interfaced to the video card by a Radio Shack rf modulator.

4. *The Master Clock.* The master clock is a crystal oscillator operating at 6.144 MHz and is generated by a 74LS00 U21 IC. This crystal frequency was chosen to display an active picture time of 42 microseconds. The initialization software of the 6845 is used to fine-tune this display time. A counter is used to divide the clock frequency by 2 and 4.

5. *The Internal Data and Address Bus.* The entire card is designed to display an SSTV picture continuously. Since the card must be powered by an external source different from the computer, power can be dropped on the computer and the display will still be active.

When a picture is to be displayed on the card, the refresh process is interrupted for a few microseconds. This causes a small white line to appear on the display. The direct memory access (DMA) scheme used on the card is very simple in principle. Normally the addressing of RAM is from the VDG through two tri-state buffers, U16 and U17. When the CPU writes to RAM, not-RAM select is brought low and the RAM address is generated by two counters, U10 and U11. At this time, VDG buffers U12 and U13 are floated on the address bus and the counter buffers drive the bus. After the RAM has been written, the counter advances to the next address.

```
                  * ASSEMBLER CODE EXAMPLE OF TRANSMISSION OF
                  * A SSTV PICTURE OVER AMATEUR RADIO USING A
                  * TRS-8ØC COLOR COMPUTER
                  *
                          OPT PAG
Ø6ØØ                      ORG $Ø6ØØ
                  * EQUATES
             FF45 PORT2   EQU $FF45     DISPLAY A PIXEL
             FF44 PORT3   EQU $FF44     RESET HARDWARE COUNTER
             1ØØØ START   EQU $1ØØØ     DUMMY START ADDRESS OF PICTURE INFO
             FF2Ø PIA     EQU $FF2Ø     DAC PORT (CASSETTE OUTPUT)

Ø6ØØ BE   1ØØØ    XMIT    LDX #START    START ADDRESS TO XMIT
                  * FIRST DISPLAY PICTURE ON THE SCREEN
Ø6Ø3 B7   FF44            STA PORT3     RESET HARDWARE COUNTER
Ø6Ø6 A6   8Ø      XMIT1   LDA Ø,X+      GET A PIXEL
Ø6Ø8 B7   FF45            STA PORT2     DISPLAY IT ON CARD
Ø6ØB 8C   5ØØØ            CMPX #START+$4ØØØ LAST BYTE OF DISPLAY ?
Ø6ØE 26   F6              BNE XMIT1
Ø61Ø 1ØBE Ø655            LDY #TABLE    ADDRESS OF PIXEL TABLE
Ø614 7F   Ø666            CLR LINE      CLEAR LINE COUNTER
Ø617 7F   Ø665            CLR PIXC      CLEAR PIXEL COUNTER
Ø61A 8E   1ØØØ            LDX #START    START OF PICTURE RAM
Ø61D 8D   33              BSR XVERT     XMIT A VERTICAL SYNC PULSE
Ø61F A6   8Ø      XMIT2   LDA Ø,X+      GET A PIXEL
Ø621 34   Ø2              PSHS A        SAVE IT ON THE STACK
Ø623 44                   LSRA          FORMAT PIXELS FOR TRANSMISSION
Ø624 44                   LSRA
Ø625 44                   LSRA
Ø626 44                   LSRA
Ø627 A6   A6              LDA A,Y
Ø629 B7   FF2Ø            STA PIA       XMIT A PIXEL
Ø62C 35   Ø2              PULS A        GET BACK ORIGINAL TWO PIXELS
Ø62E 84   ØF              ANDA #$ØF     MASK OUT HIGH ORDER NIBBLE
Ø63Ø 8D   22              BSR DELAY     DELAY LOOP BETWEEN PIXELS
Ø632 A6   A6              LDA A,Y
Ø634 B7   FF2Ø            STA PIA       XMIT NEXT PIXEL
Ø637 8D   1B              BSR DELAY     DELAY A PIXEL
Ø639 7C   Ø665            INC PIXC
Ø63C B6   Ø665            LDA PIXC
Ø63F 4D                   TSTA          IS IT THE LAST PIXEL ?
Ø64Ø 26   C4              BNE XMIT1
Ø642 7F   Ø665            CLR PIXC      RESET PIXEL COUNTER
Ø645 8D   ØC              BSR XHORIZ    XMIT A HORIZONTAL SYNC
Ø647 7C   Ø666            INC LINE
Ø64A B6   Ø666            LDA LINE      GET NEW LINE COUNT
Ø64D 81   8Ø              CMPA #128     LAST LINE ?
Ø64F 26   B5              BNE XMIT1     NOT LAST LINE
Ø651 39                   RTS           RETURN TO MAIN LINE CALL
                  *
                  * XMIT SYNC PULSES - VERTICAL SYNC WILL BE
                  * 5Ø MILLISECONDS IN DURATION, THE HORIZONTAL
                  * SYNC PULSE WILL BE 5 MILLISECONDS IN DURATION
                  *
Ø652 39           XVERT   RTS           DUMMY ROUTINE
Ø653 39           XHORIZ  RTS           DUMMY ROUTINE
                  *
                  * PIXEL DELAY ROUTINE DELAY A SUFFICIENT AMOUNT
                  * OF TIME BETWEEN PIXELS TO XMIT THE CORRECT
                  * HORIZONTAL SYNC FREQUENCY
                  *
Ø654 39           DELAY   RTS           DUMMY ROUTINE
                  *
                  * PIXEL LOOK UP TABLE. CORRECT PIXEL BIT PATTERNS
                  * WILL BE ACCESSED IN THIS ROUTINE TO PLACE A
                  * A VOLTAGE ON THE SSTV MODULATOR TO PROVIDE THE
                  * APPROPRIATE VOLTAGE F=WHITE 23ØØ HZ.
                  * Ø=BLACK 15ØØ HZ
                  *
Ø655              TABLE   RMB 16        16 BYTES OF DATA
                  *
                  * COUNTERS IN RAM
Ø665 ØØ           PIXC    FCB Ø
Ø666 ØØ           LINE    FCB Ø
                  *
                          END XMIT
```

*Fig. 7. Program example for SSTV transmission.*

6. *Display Data.* The digital display data is latched from the data bus at the correct time by the 74LS374 U24; the black and white is twice the rate of the color. The 74LS374 U39 is latched from the data bus every 650 nanoseconds. This data is fed to both the black and white and color modulators. A multiplexer is used to feed the black and white modulator. The multiplexer 74LS157 U30 is clocked at a rate of 325 nanoseconds, which is 256 pixels per line of SSTV.

7. *Black and White Modulator.* The black and white modulator is fed from the multiplexer, U30, which feeds first the 4 low-order bits (nibbles) then the high-order nibble. The output of the multiplexer is connected to a simple digital-to-analog converter (D/A) which consists of a transistor and 10 resistors.

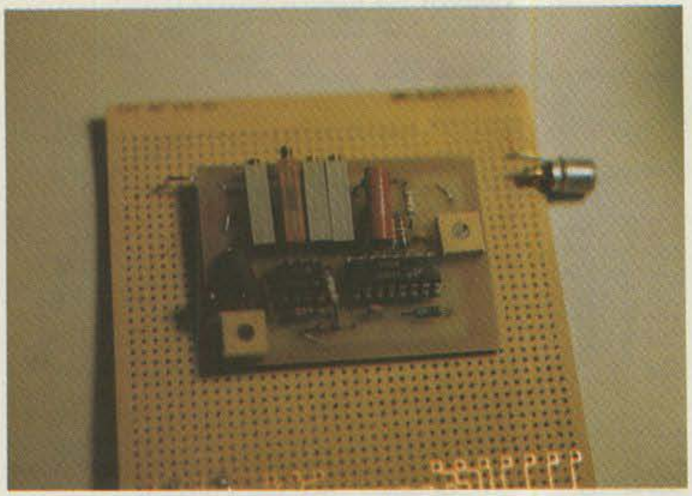

*Photo E. RTM Circuit Board's SSTV transmit interface placed on a Tandy prototype card. The card can be plugged into a card cage or a socket for ease of removal and repair.*

Sync pulses are generated by the VDG U13, are ORed together by U27, then mixed with video data in the single-transistor D/A converter. Since 4 bits are used, the modulator is restricted to 16 possible gray levels per pixel.

A picture-smoothing capacitor (1000 pF) was placed across the 510-Ohm resistor to ground at the D/A summing point. The value of this capacitor can be optimized to produce the picture most desirable. The absence of the capacitor produces a more digitized picture.

8. *Color-SSTV Modulator.* The color-SSTV modulator consists of three ICs, LM1889 U32, LM1886 U31, and a 9602 U33. The SSTV modulator functions by clocking the picture data on the latch. The data is next transferred to the LM1886 which converts the digital pixels to difference and luminance signals. These signals are internally connected to the color modulator which provides composite color video.

Three additional signals are provided to the LM1886, blanking, sync pulse, and a burst gate. The burst gate is developed from a 9602 which is a dual single shot. The burst gate serves as a reference signal. The location of the burst gate must be adjusted to the correct position on the horizontal-blanking back porch. This is the only adjustment on the board.

```
                      * ASSEMBLER CODE EXAMPLE TO INITALIZE THE CRT
                      * CONTROLLER TO THE APPROPRIATE RATES OF STANDARD
                      * USA 525 LINE TV AND NTSC COLOR TV
                      * SLIGHT MODIFICATIONS WILL ALLOW FOR 5Ø HZ
                      * 625 LINE AND PAL COLOR
                      *
                              OPT PAG
Ø6ØØ                          ORG $Ø6ØØ

Ø6ØØ 5F               INCRT   CLRB
Ø6Ø1 3Ø   8D ØØØE             LEAX CONCRT,PCR CRT INITALIZATION CONSTANTS
Ø6Ø5 F7   FF4Ø        INCRT1  STB PORT        SELECT REGISTER ADDRESS IN 6845
Ø6Ø8 A6   8Ø                  LDA Ø,X+        GET FIRST CONSTANT
Ø6ØA B7   FF41                STA PORT1       PUT DATA INTO REGISTER
Ø6ØD 5C                       INCB            POINT TO NEXT REGISTER
Ø6ØE C1   1Ø                  CMPB #16        LAST BYTE ?
Ø61Ø 26   F3                  BNE INCRT1      DO IT AGAIN
Ø612 39                       RTS
                      *
             FF4Ø     PORT    EQU $FF4Ø       CRT CONTROLLER ADDRESS PORT
             FF41     PORT1   EQU $FF41       CRT CONTROLLER DATA PORT
                      *
                      * CRT CONTROLLER IC EQUATES
Ø613 CØ               CONCRT  FCB $CØ         REG 1  HORIZ TOTAL
Ø614 8Ø                       FCB 128         REG 2  CHAR/ROW
Ø615 92                       FCB $92         REG 3  HSYNC POSITION
Ø616 1E                       FCB $1E         REG 4  HSYNC WIDTH
Ø617 78                       FCB $78         REG 5  VERT TOTAL
Ø618 35                       FCB $35         REG 6  VERTSYNC ADJ
Ø619 7F                       FCB $7F         REG 7  CHAR ROWS/FRAME
Ø61A Ø1                       FCB $Ø1         REG 8  VSYNC POS
Ø61B ØØ                       FCB Ø           REG 9  INTERLACE MODE
Ø61C Ø1                       FCB 1           REG 1Ø  SCAN LINES/ROW
Ø61D ØØ                       FCB Ø           REG 11  CURSOR START
Ø61E ØØ                       FCB Ø           REG 12  CURSOR END
Ø61F Ø2                       FCB Ø2          REG 13  MSB START VIDEO
Ø62Ø ØØ                       FCB Ø           REG 14  LSB STOP VIDEO
Ø621 ØØ                       FCB Ø           REG 15  MSB L/P
Ø622 ØØ                       FCB Ø           REG 16  LSB L/P
                      *
                              END
```

*Fig. 8. Initialization of the display board; this is an example of how the display board 6845 can be initialized.*

The digital data to the LM1886 (U32) is in the format of 3-by-3-by-2 bits of red-, green-, blue-frame information. For example, the lower three bits of the byte are the red-frame information, the next three bits are for the green frame, and the most significant bits are for the blue frame.

This configuration allows for a possible 256 combinations which are unique colors. Since the LM1886 allows for nine bits of digital data to be inputted, the LSB is tied to the MSB of the blue-frame input of the IC to make the bit pattern compatible with the eight-bit display-data bus. This trick allows for black and white images to be displayed. Without this modification, the black and white images would have a blue hue.

9. *TV-Camera Interface.* A number of points are identified in the logic of the display-board interface for the inclusion of a TV camera at a later date. The camera interface will function as follows: When the 74LS00 U9-5 is brought low, the counter will drive the address bus. The TV-camera pixel counter will be incremented by the input U9-9. The RAM read/write is controlled by U26, and the TV-camera input at U25-12/13 will cause the RAM to switch to the write mode. Pixels can next be written to the RAM from the data bus.

## Receive Demodulator

The receive demodulator is a device which decodes the SSTV tones into a dc voltage proportional to input frequency and digital sync pulses. This circuit converts video tones of 1500 Hz and 2300 Hz to 0 volts and 5 volts, respectively. A frequency of 1200 Hz converts to a positive digital pulse.

The circuit consists of four stages of filtering and one stage of pulse shaping. Its schematic is shown in Fig. 4.

The decode by this circuit is not only compatible with SSTV but can also be used to decode FAX pictures transmitted commercially on the HF frequencies.

The SSTV video enters the demodulator through the limiter circuit, U1. The limiter is connected to two bandpass filters, U1 and U2, which have bandpasses of approximately 1100 to 2400 Hz. These filters are connected to two diode-discriminator circuits which are combined into a differential amplifier. The signal at TP2 is the carrier frequency of the audio signal with amplitude modulation. The signal in this path with TP3 (U3 and U4) is a series of bandpass amplifiers which allow only the video components of 1500 and 2300 Hz to be passed.

The path of TP4 and U4 is used for the detection and waveshaping of the sync signals. The Schmitt trigger, 7414, is used to develop fast rise times of the sync signals and to produce TTL-level voltages. The sync output from the circuit contains both horizontal and vertical sync pulses.

## Modulator Circuit

The modulator interfaces to the CoCo and is the circuit which produces the SSTV audio tones for the transfer of video information in computer memory. The interface, shown in Fig. 5, connects to the CoCo through the RS-232 and cassette-output ports. The cassette-output port is a 6-bit digital-to-analog converter.

The circuit functions as follows. When the RS-232 output is raised, the modulator outputs a sync frequency of 1200 Hz. To generate video tones, a ground

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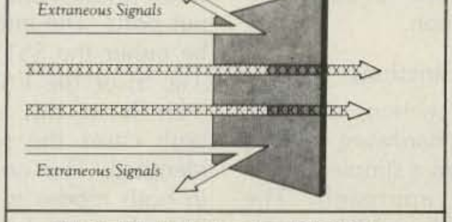


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Photo F. A color-SSTV picture displayed on a TI color monitor attached to the K6AEP prototype display board. The picture was received over amateur radio on 28.680 MHz by the TRS-80C and saved on tape. The picture was generated by WB0UNB in St. Louis, Missouri.

Photo G. A color-SSTV picture generated by W0LMD and placed on audio cassette tape and loaded into the TRS-80C. This picture shows the effect of color contouring. Since the display has only 256 possible colors, the shading in the flesh-tone regions are noticeable.

potential is applied to both the RS-232 output and the video input. This causes a video frequency of black 1500 Hz to be outputted. When the video level is increased to approximately 1.1 volts by outputting a digital F to the cassette-output port, a frequency of 2300 Hz is generated. By the use of software, an SSTV picture can be generated by software and transmitted.

**The Software**

The preceding section provides you with a complete description of the hardware requirements for SSTV applications. Obviously, the hardware performs few useful functions without the software. The intent of the hardware design is to place the burden of all timings and control on the software. This allows for the maximum utilization of all hardware interfaces. There are the following limiting factors.

*Microprocessor Speed.* The reception or transmission of images is limited by the rate at which the instructions can be executed by the CPU. Fortunately, the 6809 microprocessor is very fast due to its rich instruction set and its ability to process 16-bit data even though the processor is on an 8-bit data bus.

*Internal Analog-to-Digital Converter.* All of the preceding interfaces are based upon the use of the internal analog-to-digital converter in the TRS-80C. This feature is used to process joystick inputs when playing games. The A/D converter uses a simple successive-approximation technique and is driven by the microprocessor. When this technique is used, the conversion rate is quite slow. The tightest loop which can be written to utilize this feature allows for the conversion of 4 bits of data in approximately 75 microseconds. Even though this is slow, the rate is sufficient to allow for SSTV and FAX reception.

**Software Functions**

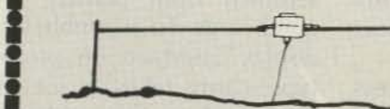
In this section, the software and hardware will be described in a simple, broad, overview approach. The principles described can apply to SSTV, FAX, or any other communications mode which uses a slow rate of transmission or reception. Normally this type of software is called firmware or microcode. Since the software is extremely time-dependent, care must be taken with each instruction written to make the time as short as possible. The description of the software routines will be general enough so that they can be recoded for any general-purpose microprocessor. One important point is that all software must be written in the microprocessor's native assembler language. High-level languages are too slow. Even the most efficient compilers are too slow for SSTV applications.

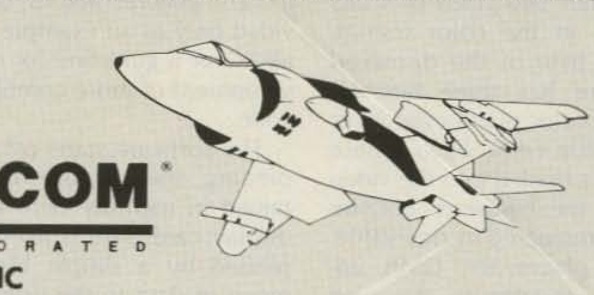
*Receive Software.* In Fig. 6 is a simple routine which will receive a picture through an interface attached to the CoCo joystick and RS-232 input ports. The interface can be either the SSTV receiver (Fig. 5) or the FAX receiver (Part II of this article). In both cases the software is identical. The only change in both modes is the delay between pixel reception. The software routines provided are not complete but they do provide an example to readers ambitious enough to learn assembler-language programming. The program functions as follows.

The first six lines of code initialize program constants for the correct number of lines and place the CoCo multiplexer to the correct joystick-input-connector pin. The hardware counter PORT3 is reset to the upper left-hand corner of the picture area. As soon as a vertical sync signal is received on the interface, the program starts to digitize the picture.

The A/D routine converts the analog input voltage to four digital bits and places this information into the lower nibble of a byte. The byte is next placed on the stack, and a software delay is executed. Upon completion of this delay, the next A/D reading is converted. These two values are next added together on the stack, then placed into RAM, and simultaneously displayed on the video card.

The byte in RAM is the same format as the byte on the video card. In the black and white format, the byte





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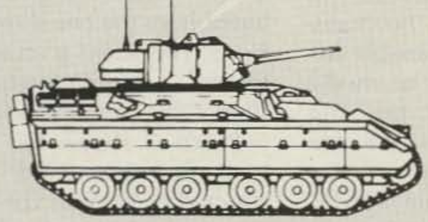

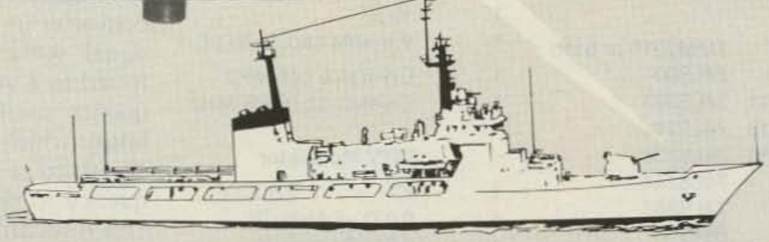

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contains two pixels of 4 bits each. In the color format, each byte of the displayed picture has three bits for each color plane except for the blue color. Each time a byte is loaded into the video port, the hardware counter is incremented by one value. This places the DMA address counter to the next location in RAM where the next pixel will be written.

*Transmit Software.* Fig. 7 contains a simplified example of how an SSTV transmit routine can be written. This example, like SSTV receive, is very general and is provided only as an example to allow for a guideline for development of more complex code.

The software starts off by placing the picture contained in memory onto the display card. This is accomplished by a simple block move of data to the display card. Prior to the block move, the card hardware counter is reset to zero and 16K bytes are taken from RAM and transferred to the video card. Each time the byte is stored at the video-card address, the hardware automatically increments the RAM address to the next location.

The transmission process starts off by issuing a vertical sync pulse. This pulse allows for the receiver on the other end of the transmission path to reset the picture to the top of the screen. In the following steps, a picture byte in memory is loaded into the A accumulator. Each nibble is formatted into the lower nibble of a byte. This byte is next used as an offset to a lookup table in memory which will convert the address to an appropriate digital signal which can be transferred to the D/A converter in the CoCo. This signal will then be transferred to a vco (variable frequency oscillator or modulator) which converts this signal to a sinusoidal frequency in the audio range. This resultant signal is SSTV.

The program continues to transmit pixels until 256 pixels are transmitted. At this time a horizontal sync pulse is transmitted. The program next checks if 128 lines have been transmitted. If so the whole process is terminated. If not, the program continues to transmit pixels.

*CRT Controller Initialization.* Fig. 8 contains a software routine which will initialize the 6845. The routine takes 16 bytes of data in the table CONCRT and stuffs them into the controller registers. This process is accomplished by first presenting the controller register number to the IC. Next the data byte is loaded into the accumulator then transferred to the card.

The display constants in CONCRT are for a standard 60-Hz display system. To revise the formats to 50 Hz, 625 lines, registers 1 and 5 must be changed. The values should be selected by trial and error.

## Hardware Construction

The hardware mentioned above can be constructed on prototype cards or assembled from printed circuit boards. To assemble the display interface on prototype cards takes a lot of work and is vulnerable to errors. Problems experienced with prototyping the card have included: grounds conductors were too small, too few bypass capacitors on power lines, and hardware counters U10 and U11 required a small capacitor on the counter-reset line. Despite these problems, about 5 boards have been constructed to date with excellent results.

Photo A shows the multimode display board.[1] This interface is very compact and its design is slightly different from the one shown in Fig. 3. The board is attached to the computer through a short cable (see Photo B).

Photo C shows the original prototype card constructed by K6AEP. The card was point-to-point solder-wired on a prototype SS-50 computer interface card. A small adapter card was constructed to plug into the CoCo expansion interface. (An etched PC board or completely assembled version of this card is available from L. W. InterFace.[3]

The SSTV receive and transmit interfaces are available in a number of forms. Photo D shows the multimode receive-board interface card; Photo E is a transmit interface from RTM Circuit Boards.[2]

All boards can be placed in a cabinet with the appropriate power supplies of 5 volts (1 Amp) and ±12 volts (100 mA). Cables can be made to attach to the computer and receivers.

Part II of this article will describe the FAX hardware.

## Conclusions

The computer approach to displaying images is a very cost-effective method. Most alternative methods available are limited in function and are considerably more costly. The commer-

### Parts List

**Display Board**

| | | |
|---|---|---|
| **ICs** | | |
| 8 | U1–U8 | TMM2016 or 6116 |
| 1 | U9 | 74LS00 |
| 2 | U10, U11 | 74LS393 |
| 2 | U12, U13 | 74LS244 |
| 2 | U14, U15 | 74LS138 |
| 1 | U16 | 74LS244 |
| 1 | U17 | 74LS367 |
| 1 | U18 | 6845 |
| 1 | U19 | 744LS93 |
| 1 | U20 | 74LS245 |
| 1 | U21 | 74LS00 |
| 1 | U22 | 74LS11 |
| 1 | U23 | 74LS367 |
| 1 | U24 | 74LS02 |
| 1 | U25 | 74LS00 |
| 1 | U26 | 74125 |
| 1 | U27 | 74LS02 |
| 1 | U28 | 74LS05 |
| 1 | U29 | 74LS374 |
| 1 | U30 | 74LS157 |
| 1 | U31 | LM1886 |
| 1 | U32 | LM1889 |
| 1 | U33 | 9602 |
| **Transistors** | | |
| 2 | 2N3904 | |
| **Resistors** | | |
| 1 | 75 Ohms | ¼ W, 5% |
| 2 | 150 | ¼ W, 5% |
| 2 | 220 | ¼ W, 5% |
| 2 | 470 | ¼ W, 5% |
| 1 | 510 | ¼ W, 5% |
| 1 | 600 | 1/10 W, 1% |
| 1 | 680 | ¼ W, 5% |
| 8 | 1k | ¼ W, 5% |
| 1 | 1.2k | 1/10 W, 1% |
| 1 | 2.4k | 1/10 W, 1% |
| 1 | 4.7k | ¼ W, 5% |
| 1 | 5.1k | 1/10 W, 1% |
| 2 | 5.1k | ¼ W, 5% |
| 1 | 10k | ¼ W, 5% |
| 2 | 50k Trimpot | |
| **Capacitors** | | |
| 3 | 43 pF | Mica |
| 2 | 100 pF | Mica |
| 1 | 1000 pF | Mica |
| 1 | 0.001 μF | |
| 1 | 0.01 μF | |
| 20 | 0.1 μF | |
| 1 | 10 μF | |
| 1 | Variable cap, 9–35 pF | |
| 1 | Crystal, 6.144 MHz | |
| 1 | Crystal, 3.579545 MHz | |

**SSTV Modulator**

| | | |
|---|---|---|
| 1 | IC | XR 2206 |
| 1 | 0.033 μF Mylar™ | |
| 1 | 0.01 μF Ceramic | |
| **Resistors** | | |
| 2 | 200 Ohms | ¼ W, 5% |
| 2 | 5.1k | ¼ W, 5% |
| 1 | 10k | ¼ W, 5% |
| 1 | 22k | ¼ W, 5% |
| 1 | 39k | ¼ W, 5% |
| 1 | 47k | ¼ W, 5% |
| 1 | 1k | Trimpot |
| 1 | 5k | Trimpot |
| 1 | 50k | Trimpot |

**SSTV Receive Interface**

| | | |
|---|---|---|
| 4 | IC 1–4 | MC1458 |
| 1 | IC5 | 7414 |
| **Resistors** | | |
| 1 | 620 Ohms | ¼ W, 5% |
| 2 | 1.0k | ¼ W, 5% |
| 1 | 2k | ¼ W, 5% |
| 4 | 4.7k | ¼ W, 5% |
| 11 | 10k | ¼ W, 5% |
| 3 | 15k | ¼ W, 5% |
| 2 | 18k | ¼ W, 5% |
| 1 | 20k | ¼ W, 5% |
| 3 | 39k | ¼ W, 5% |
| 3 | 82k | ¼ W, 5% |
| 1 | 220k | ¼ W, 5% |
| 1 | 4.7 M | ¼ W, 5% |
| 1 | 1k | Trimpot |
| 1 | 10k | Trimpot |
| **Capacitors** | | |
| 3 | *0.0047 μF Mylar™ | |
| 1 | *0.01 μF Mylar | |
| 6 | *0.022 μF Mylar | |
| 2 | *0.068 μF Mylar | |
| 1 | *25 μF Mylar | |
| **Small Signal Diodes** | | |
| 8 | *1N914 | |

* Or equivalent.

cial units have one advantage in that they can be purchased and plugged into the wall and they are operational. The computerized system described takes a little more work, but it is extremely flexible and not subject to obsolescence as are its commercial counterparts. The results achieved with the system described here rivaled those of commercial counterparts.

Photo F is a typical color image, 128 pixels per line on 128 lines, 256 colors per pixel. Photo G is another color-SSTV image which shows the resolution of the display board on facial flesh tones. This type of image is the hardest type to display. This picture shows color contouring due to the 256 colors per pixel. Photo H is another color picture with computer-graphics overlays generated by software. The picture is the same as Photo G but reduced in size by one half. The colored image was moved to the center of the display screen and graphical characters of various colors were distributed around the picture.


*Photo H. A color-SSTV picture with graphics. This picture is the same as Photo G, but reduced in size by software and placed in the center of the image area. The graphics were generated by software and placed around the picture. The graphics and picture were all generated by the K6AEP SSTV 7.6 Revision 2 program.*

Better results can be achieved with 32K of display memory, but photos were not presented in this article for this mode. The black and white images developed by this display density approach fast-scan TV quality.

More photos will be presented in Part II of the article, on the FAX application.

Obviously a project of this magnitude is not a one-person effort. Some of the people who contributed were Ron Adair K5HFT of Multimode Corporation, Bob Blackstock WB5MRG who helped with the display-board design, Larry Fritz AG8O of L. W. InterFace, and Bob Wilson WBØRTM of RTM Circuit Boards. ■

**References**

[1] Multimode Corp., PO Box 171171, Arlington TX 76016; (817)-572-3996.

[2] RTM Circuit Boards, 205 Elm Street, Van Horne IA 52346-0400.

[3] L. W. InterFace, 9570 Kinsman Road, Novelty OH 44072.